WHAT IS CLAIMED IS:

1. An integrated services digital network private branch exchange, which is capable of automatically choosing a synchronization clock source, comprises:

a plurality of priority selection circuits that are connected each other in a daisy chain circuit manner for sending out a frame-synchronization clock output signal and a data clock output signal;

a plurality of trunk chips that are connected to a network terminal via a truck interface, and then connected to a central office via the network terminal for receiving the frame-synchronization clock output signal and the data clock output signal; and

a plurality of subscribe chips that are connected to a terminal equipment via a subscribe interface for receiving the frame synchronization clock output signal and the data clock output indication signal.

2. The integrated services digital network private branch exchange of claim 1, wherein each priority selection circuit of the priority selection circuits comprises:

a first NOT gate, has an input port of the first NOT gate that is connected to an active level of a layer 1 of one of the LT-T chips, and an output port of the first NOT gate;

a second NOT gate, having an input port of the second NOT gate that is connected to a privilege level signal, and an output port of the second NOT gate;

a first AND gate, having a first input port of the first AND gate that is connected to an external clock indication signal, a second input port of the first AND gate that is connected to the active level of the layer 1 of the LT-T chip, and an output port of the first AND gate that is connected to an internal clock output signal;

a second AND gate, having a first input port of the second AND gate that is connected to the output port of the first AND gate, a second input port of the second AND

gate that is connected to the output port of the second NOT gate, and an output port of the AND gate;

a third AND gate, having a first input port of the third AND gate that is connected to the external clock indication signal, a second input port of the third AND gate connected to the output of the first NOT gate, and an output port of the third AND gate;

an OR gate, having a first input port of the OR gate that is connected to the output port of the third AND gate, a second input port of the OR gate that is connected to the output port of the second AND gate, and an output port of the OR gate;

a clock recovery circuit, having an input port of the clock recovery circuit that is connected to a T interface, and an output port of the clock recovery circuit;

a first frequency divider, having an input port of the first frequency divider that is connected to the output port of the clock recovery circuit, and an output port of the first frequency divider;

a switch, having a first input port of the switch that is connected to a first clock signal, a second input port of the switch that is connected to the output port of the first frequency divider, a control port, a first output port of the switch and a second output port of the switch that are connected to the output port of the OR gate;

a digital phase locked loop, having a first input port of the digital phase locked loop that is connected to the first output port of the switch, a second input port of the digital phase locked loop that is connected to the second output port of the switch, a first output port of the digital phase locked loop and a second output port of the digital phase locked loop;

a second frequency divider, having an input port of the second frequency divider that is connected to the first output port of the digital phase locked loop, and an output port of the second frequency divider;

a first buffer, having an input port of the first buffer that is connected to the output port of the second frequency divider, an output port of the first buffer that is connected to a frame synchronization clock output signal, and a control port of the first buffer that is connected to the output port of the OR gate, which also connects to the control port of the switch; and

a second buffer, having an input port of the second buffer that is connected to the second output port of the digital phase locked loop, an output port of the second buffer that is connected to a data clock output signal, and a control port of the second buffer that is connected to the output port of the OR gate, which is also connected to the switch.

3. The integrated services digital network private branch exchange of claim 2, wherein the digital phase locked loop is collocated on the chip of the integrated services digital network private branch exchange is capable of automatically choosing a synchronization clock source.

4. The integrated services digital network private branch exchange of claim 1, wherein each priority selection circuit of the priority selection circuits, comprises:

a first NOT gate, logically inverts an active level of the layer 1 of one of the trunk chips to generate an output signal of the first NOT gate;

a second NOT gate, logically inverts a privilege level signal to generate an output signal of the second NOT gate;

a first AND gate, proceeds an "AND" logical operation on an external clock indication signal and the active level of the layer 1 of the trunk chip to generate an internal clock output signal;

an second AND gate, proceeds an "AND" logical operation on the internal clock output signal and the output signal from the second NOT gate to generate an output signal of the AND gate;

a third AND gate, proceeds an "AND" logical operation on the external clock indication signal and the output signal from the first NOT gate to generate an output signal of the third AND gate;

an OR gate, proceeds an "OR" logical operation on the output signal from the third AND gate and the output signal from the AND gate to generate an active level;

a clock recovery circuit, transforms a pseudo-ternary signal from a trunk interface into a second clock signal;

a first frequency divider, divides the frequency of the second clock signal to generate a third clock signal;

a switch, which is in the short circuit state when the active level is high logic level, and in the open circuit state when the active level is low logic level;

a digital phase locked loop, receives the first clock signal and the third clock signal when the switch is in the short circuit state, to generate a fourth clock signal;

a second frequency divider, divides the frequency of the fourth clock signal, to generate a fifth clock signal;

a first buffer:

when the active level is high logic level, the first buffer is activated, and the fifth clock pulse is used as a clock of the frame synchronization clock output signal; and

when the active level is low logic level, the first buffer is in the disable state; and

a second buffer:

when the active level is high logic level, the second buffer is activated, and the fourth clock signal is used as a clock of the data clock output signal; and

when the active level is low logic level, the second buffer is in the disable state.

5. The integrated services digital network private branch exchange of claim 4, wherein the digital phase locked loop locks the third clock signal that is synchronous to the central office with the first clock signal to generate the fourth clock signal that is used as the clock of the data clock output signal of the local integrated services digital network private branch exchange, whereas the fourth clock signal, via the second frequency divider, generates the fifth clock signal that is used as the clock of the frame synchronization clock output signal of the local integrated services digital network private branch exchange.

6. A method, for automatically choosing a synchronization clock source, is suitable for an integrated services digital network private branch exchange having a plurality of trunk chips and a plurality of subscribe chips, comprises the steps of:

providing a plurality of priority selection circuits; and

when one external line is called, the priority selection circuits choose a priority selection circuit and a chip having the highest priority, from the priority selection circuits

and the trunk chips, and activate a layer 1 of the trunk chip to provide a synchronization clock source that is synchronous to a central office.

7. The method of claim 6, wherein the synchronization clock source is generated by a clock recovery circuit of the priority selection circuit.

8. The method of claim 6, wherein a DPLL circuit of the trunk chips that are not chosen as the synchronization clock source, are all in the disable state.

9. The method of claim 6, wherein if no external line called, the priority selection circuits activate a priority selection circuit and a layer 1 of the chip having the lowest priority from the priority selection circuits and the chips to provide a stable free running clock.

10. A control method of the digital phase locked loop capable of automatically choosing the synchronization clock source, the method is suitable for an integrated services digital network private branch exchange having a plurality of trunk chips and a plurality of subscribe chips, comprises the steps of:

providing a plurality of digital phase locked loops that are collocated on the priority selection circuits;

when one external line is called, the priority selection circuits choose a priority selection circuit and a chip having the highest priority from the priority selection circuits and the trunk chips, and activate the layer 1 of the trunk chip to provide a synchronization clock source that is synchronous to a central office; and

locking the synchronization clock signal that is synchronous to the central office with one of the digital phase locked loops of the priority selection circuits.

11. The control method of claim 10, wherein the digital phase locked loop is in an active state.

12. The control method of claim 10, wherein the digital phase locked loops that are not chosen as the synchronization clock source are all in a disable state.

13. The control method of claim 10, wherein when no external line called, only a priority selection circuit having the lowest priority among the priority selection circuits is activated, all other digital phase locked loops are in the disable state.